[This question paper contains 8 printed pages.]

Your Roll No.....

Sr. No. of Question Paper : 841 **G**

Unique Paper Code : 2342572301

Name of the Paper : Computer System Architecture

Name of the Course : **B.A. (Prog.) Computer Science**

Semester : III

Duration : 3 Hours Maximum Marks : 90

Instructions for Candidates

1. Write your Roll No. on the top immediately on receipt of this question paper.
2. Question No. **1** in **Section-A** is compulsory.
3. Attempt any **4** questions from among questions **2** to **7** in **Section-B**.
4. Parts of a question must be answered together.

Section-A

1. (a) Give two instructions required to set E=1 in basic computer. (2)

P.T.O.

(b) State and prove associative law on the following expression using truth table.

$AB + B'C + A'C$ (3)

(c) Which addressing mode is used to implement register-reference instructions. Justify your answer. (3)

(d) Show the representation of +8 and –7 in : (3)

(i) Signed Magnitude Representation

(ii) Signed 1's complement representation

(iii) Signed 2's complement representation

(e) Explain how ROM is different from RAM and give its applications. (3)

(f) The 8-bit registers AR, BR, CR, and DR initially have the following values: (4)

AR = 11110010

BR = 11111111

CR = 10111001

DR = 11101010

Determine the 8-bit values in each register after the execution of the following sequence of microoperations.

$CR \leftarrow CR \wedge DR$, $BR \leftarrow BR+1$ AND DR to CR, increment BR

$AR \leftarrow AR-CR$ Subtract CR from AR

(g) Implement OR and AND gates using only NAND gates. (4)

(h) Give reason why : (4)

(i) $SC \leftarrow 0$ is written at the end of execute sequence of all instructions.

(ii) $IR \leftarrow M[PC]$ is not valid.

(i) Draw the diagram representing the I/O buses and Interface-modules. (4)

Section-B

2. (a) Given the Boolean function (10)

$$F = xyz' + x'y'z + x'y'z'$$

(i) List the truth table of the function.

(ii) Draw the logic diagram using the original Boolean expression.

(iii) Simplify the algebraic expression using Boolean algebra.

(iv) List the truth table of the function from the simplified expression and show that it is same as the truth table in part i.

(v) Draw the logic diagram from the simplified expression and compare the total number of gates with the diagram of part ii.

(b) Simplify the Boolean function F together with don't care conditions d in sum of products (SOP) form. Also draw the logic diagram of the simplified expression.

$F(w,x,y,z) = \Sigma(1, 2, 5, 7, 8, 10)$

$d(w,x,y,z) = \Sigma(3, 6, 11, 15)$

(5)

3. (a) The memory unit is specified by the number of words times the number of bits per word. How many address lines and input-output data lines are needed for 8 M X 32 memory unit? Also draw its diagram. (5)

(b) Explain the designing of a 2-to-4-line decoder implemented using NAND gates. (6)

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(c) Explain 4-bit binary adder using the logic diagram. (4)

4. (a) Write the micro-operations for implementing the following memory reference instructions of basic computer.

(i) Direct STA

(ii) Indirect BUN

(iii) Direct ISZ (6)

(b) The content of PC in the basic computer is 2A8 (all numbers are in hexadecimal). The content of AC is 7E02. The content of memory at address 2A8 is 935C. The content of memory at address 35C is 07AB. The content of memory at address 7AB is 219 A. (9)

(i) What is the instruction that will be fetched and executed next?

(ii) Show the binary operation that will be performed in the AC when the instruction is executed.

(6)

(iii) Go over the instruction cycle to perform the above operation and give the contents of registers PC, AC, AR, DR, IR, I at the end of execute cycle.

5. (a) Covert the following decimal numbers to the base indicated. (2+2+2)

(i) 7562 to octal

(ii) 1938 to hexadecimal

(iii) 175 to binary

(b) Write the formula to find the (r–1)'s complement. Find the 7's complement of $(2345)_8$. (3)

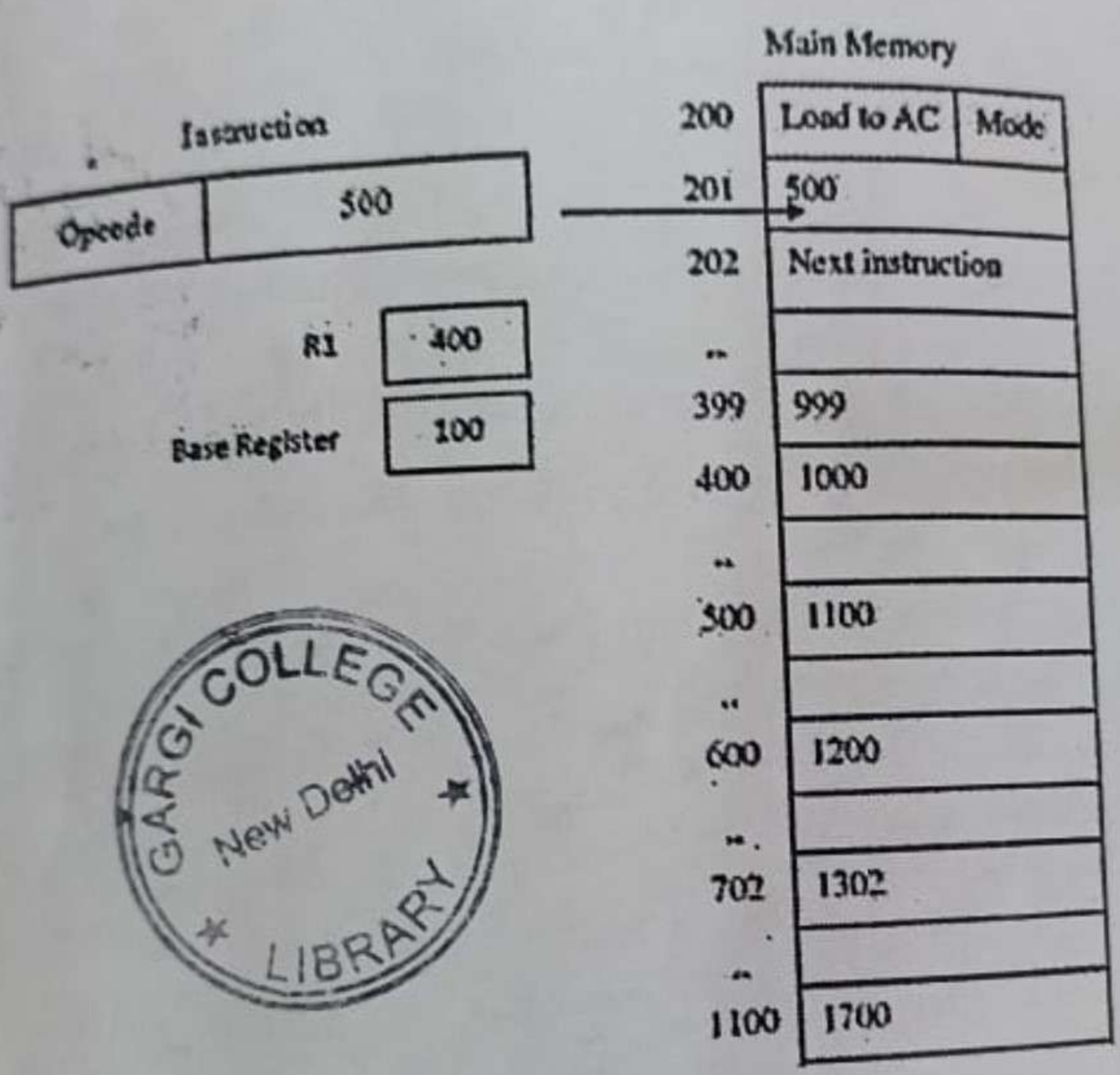
(c) Perform the following arithmetic operations using 7-bit registers and detect the overflow, if any :

(+42) + (+33) and (–42) –(+33)

Use signed 2's complement representation for negative numbers. (6)

6. (a) A two-word instruction to perform the load operation is stored in memory at an address 200 as represented in the memory map given below.

The address field of the instruction is stored at address 201. The mode field specifies an addressing mode. R1 is the general purpose register, which has the value of 400. Base register contains the value 100.



Determine the effective address and the operand to be loaded for the following address modes :

(i) Direct

(ii) Immediate

(iii) Indirect

(8)

(iv) Relative

(v) Base register Addressing

(vi) Register indirect addressing

(b) Demonstrate how interrupt is handled by drawing the memory diagram before and after the execution of an interrupt. (12)

7. (a) Differentiate between (attempt any **two**) : (3)

(i) Programmed I/O and Interrupt driven I/O techniques

(iii) Main memory and Auxiliary memory

(iii) Isolated vs Memory mapped I/O (6)

(b) Explain data transfer from I/O device to CPU in programmed I/O with the help of suitable diagram and flow chart. (9)

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Semester : III

Duration : 3 Hours Maximum Marks : 90

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Section–A

1. (a) Demonstrate the validity of the following identities by means of truth tables :

$x + y.z = (x + y).(x + z)$ (3)

P.T.O.

(b) Perform the following conversions :

(i) $(218.39)_9$ to $(\_)_{10}$

(ii) $(234)_{10}$ to $(\_)_{12}$

(c) How can you obtain a T flip-flop from JK flip-flop? Demonstrate using block diagram. (3)

(d) The state of a 12-bit register is 100010110111. What is its content if it represents : (3)

(i) The decimal digits in BCD representation

(ii) The decimal digits in Binary coded octal representation

(iii) The decimal digits in Binary coded hexadecimal representation (3)

(e) Simplify the following Boolean expression to minimum number of literals using Boolean algebra :

$$(BC' + A'D)(AB' + CD') \quad (3)$$

(f) The binary adder-subtractor circuit has the following values for the input-mode M and the data input A and B. Determine the values of the outputs S_3, S_2, S_1, S_0, and the carries generated i.e. C_4, and C_0.

$M = 1,\ A = 1011,\ B = 0101$ (3)

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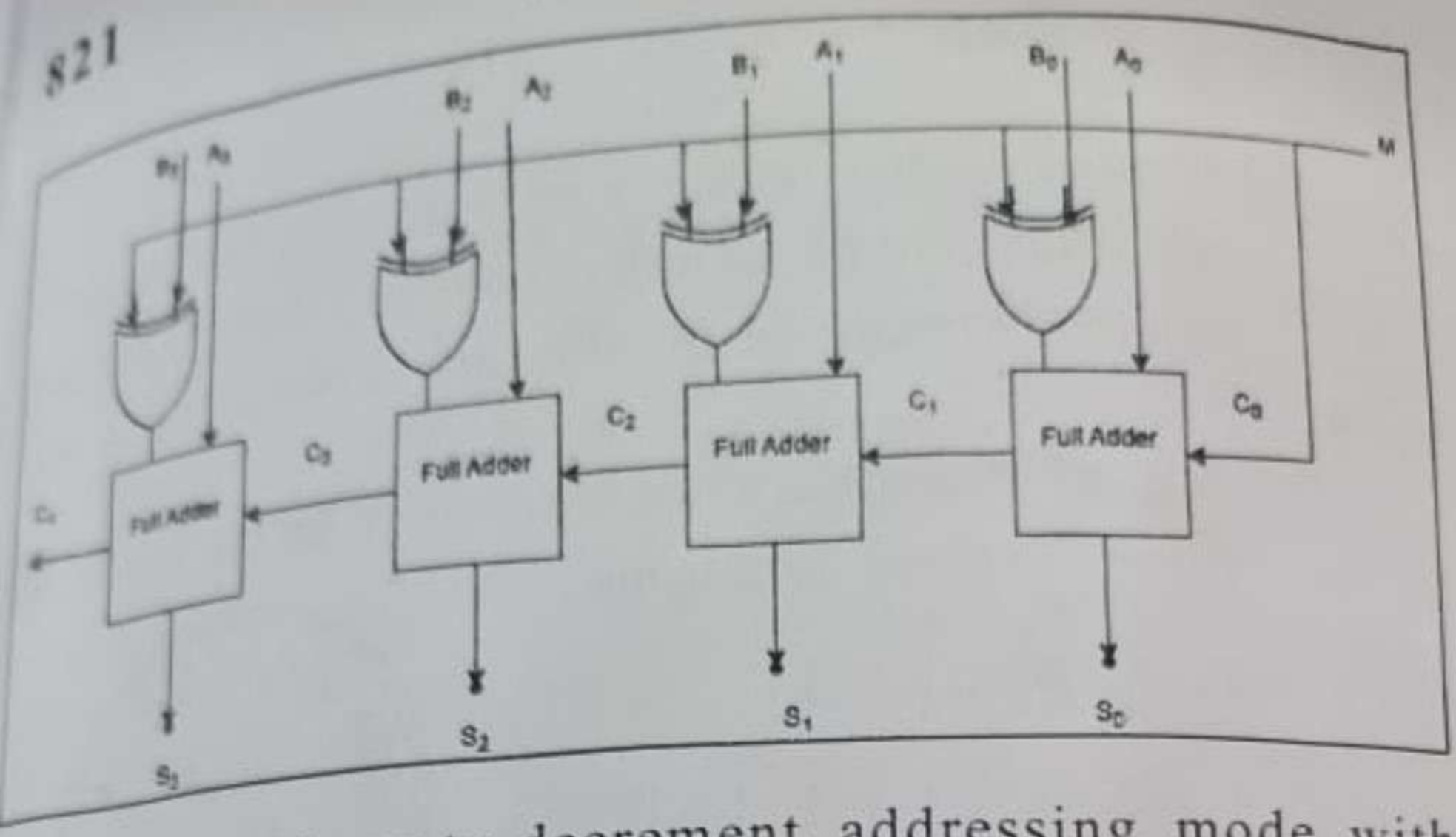

(g) Explain auto-decrement addressing mode with examples. (3)

(h) Explain the "branch and save return address" operation with the help of a memory diagram. (3)

(i) Explain the importance of following condition bits:

(i) FGO-flag

(ii) E-flag

(iii) I-flag (3)

(j) Differentiate between half adder and full adder with the help of an example. (3)

Section–B

(a) Simplify the following Boolean expression in sum-of-product (SOP) using K-map form and draw the logic diagram of the simplified expression.

$(A' + C)(A' + C')(A+B+C'D)$

(b) Describe what happens during an interrupt cycle with the help of memory diagram? Also Write the micro-instructions for the interrupt cycle. (4) (5)

(c) A combinational circuit is specified by the following three Boolean functions :

$F_1(A, B, C) = \Sigma(3, 5, 6)$

$F_2(A, B, C) = \Sigma(1, 4)$

$F_3(A, B, C) = \Sigma(2, 3, 5, 6, 7)$

Construct the truth table for the above-mentioned circuit and implement the circuit with a decoder constructed with NAND gates. (6)

3. (a) Differentiate between combinational and sequential circuits and give two examples of each. (2+2)

(b) Perform the following arithmetic operations with binary numbers in signed 2's complement representation. Use 8-bit to accommodate each operand along with its sign. Identify in each case, if this operation results in overflow or not.

(i) (–75) + (–45)

(ii) (–75) + (+45) (2+3)

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(c) Write the micro-instructions for the execute sequence of following machine instructions:

(i) Indirect mode STORE

(ii) Direct mode ISZ

(iii) Indirect mode BUN (6)

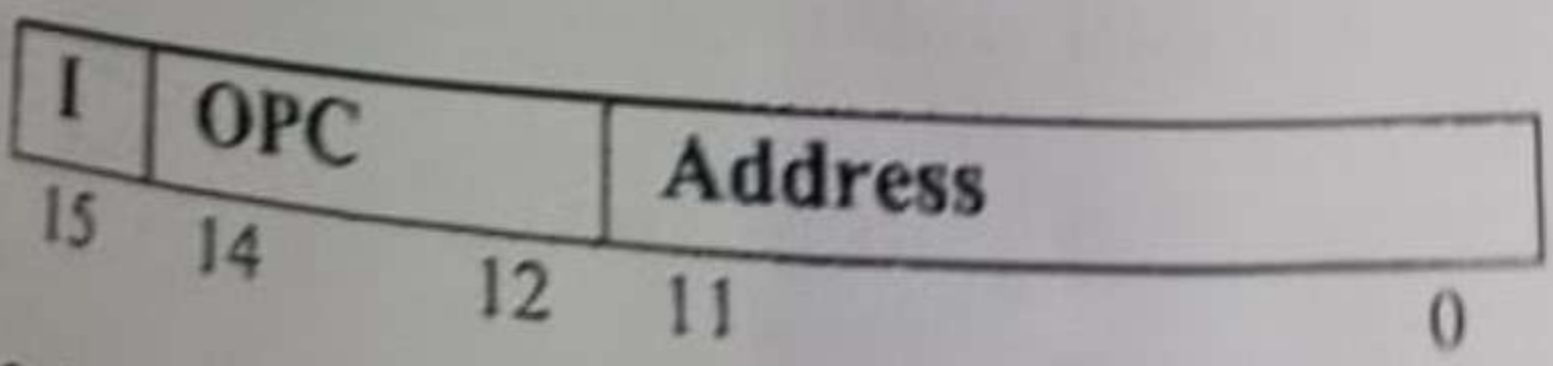
4. (a) What is meant by bus request and bus grant with respect to direct memory access? (2)

(b) (i) Perform subtraction on the given unsigned numbers using the 10's complement of the subtrahend :

6428 – 3409

(ii) Construct the characteristic table for SR flip-flop. (3+2)

(c) The initial content of PC is 120. The content of memory at 120 is C1A0. The content of the memory at 1A0 is 0250. The content of memory at address 250 is 0134. Assuming the instruction has the format as mentioned below :



And 3-bit opcode for BUN is $(100)_2$ and BSA is $(101)_2$.

(i) Specify the instruction that will be executed next and the addressing mode to be used.

(ii) Specify the micro-instruction to be execute sequentially for the fetch and execute sequence for the given instruction

(iii) Show the contents in hexadecimal of registers PC, AR, DR, IR, and SC of the basic computer.

Give the answer in a table with 6-columns. Column-1 must contain the micro-instructions (response of part ii). Column 2-6 must display the contents for each register and a row for each timing signal. Show the content of registers after the positive transition of each clock-pulse. (8)

5. (a) Explain Index-register addressing mode with the help of an example. Also specify when/ where is it used. (4)

(b) Assuming the given data stored in 8-bit register. Perform the following operations and represent the result obtained in hexadecimal :

$A = (7C)_{16}$, $B = (65)_{16}$

(i) A (AND) B

(ii) A (XOR) B

(iii) 2's complement of B

(iv) A – B

(v) Circular Shift right 2 times A. (5)

(c) A computer uses a memory unit of 64M words of 36-bits each. A binary instruction code is stored in one word of the memory. The instruction has four parts :

(i) An addressing mode field to specify one of the four-addressing modes,

(ii) Operation code,

(iii) A register code part to specify one of the 14 registers and an address part.

How many bits are there in addressing mode part, opcode part, register code part, and the address part? Draw the instruction format, clearly specifying the indexes and the number of bits for each part. (6)

(a) Represent $(-84)_{10}$ in 10 bits register using following representation :

(i) Sign-magnitude representation

(ii) 1's complement Representation

(iii) 2's complement representation. (4)

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(b) How many address lines, data input lines and data output lines are present in a memory unit represented by 4096×16? How many 256×8 memory chips are needed to provide a memory capacity of 4096×16? (5)

(c) A two-word instruction is stored at location 500 with its address field at location 501. The address field has the content as 600. The content of memory word at address 600 is 650. A processor register R1 contains the number 300. Evaluate the effective address if the addressing mode of the instruction is

(i) Immediate (ii) Direct

(iii) Indirect (iv) Relative

(v) Register-indirect

(vi) Indexed with R1 as the index-register. (6)

7. (a) Draw the flowchart for the execute sequence of all memory reference instructions along with the control conditions. (6)

(b) Write short notes **(any three)** :

(i) Memory mapped I/O

(ii) ISZ instruction

(iii) Register reference Instructions

(iv) Octal to decimal decoder (9)